MULTIPORT COMMUNICATIONS INTEGRATED CIRCUIT

TECHNICAL FIELD

[0001] This invention relates to integrated circuits, and more particularly to integrated circuits for interfacing to computer peripheral devices.

BACKGROUND

[0002] Performance increases in computers are generally related to the evolution of components and assemblies such as memory, hard drives, processors, and graphics accelerators. Somewhat lagging in evolution has been the bus that is employed for interconnecting the components and assemblies of computers. Recently, several new standards for next generation high speed buses have been proposed. In addition, a new standard (Serial ATA) for interconnecting computer systems to internal storage units has been proposed. These new standards offer the promise of further increases in performance, but also present a new set of problems in creating workable interconnect designs.

SUMMARY

[0003] An integrated circuit for multi-port communications is provided. The integrated circuit includes a high speed bus interface to interface to a core chipset through a high speed

bus. A serial mass data storage host adapter is in communication with the high speed bus interface to control a high speed mass data storage unit. A network controller is in communication with the high speed bus interface to control a network port.

[0004] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0005] FIG. 1 is a block diagram of a conventional computer bus structure.

[0006] FIG. 2 is a block diagram of an embodiment of a multi-port communications chip coupled to a core chipset.

[0007] FIG. 3 is a block diagram of a high speed Ethernet controller.

[0008] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0009] Shown in Figure 1 is a block diagram of one conventional computer bus structure. The computer system core

components comprising a processor 10, memory 11, and graphics device 12 may be connected to the peripheral components through a core chipset 13. The core chipset 13 typically includes a memory bridge 14 to control memory accesses, an accelerated graphics processor 15 to control graphics operations, and an I/O bridge 16 to control the flow of information over a local bus between the processor 10 and the peripheral devices. The I/O bridge 16 typically includes a parallel ATA host adapter 17 to connect a storage device 9 to the processor 10 over the local bus. A PCI controller 18 controls access to the local bus by I/O devices such as a network controller 19.

[0010] Shown in Figure 2 is a block diagram of an embodiment of a multi-port communications chip 20 coupled to a core chipset 22. The multi-port communications chip 20 advantageously provides control for a serial ATA port 24 as well as a high speed Ethernet port 26 on a single integrated circuit that is outside of the core chipset 22. The integrated circuit is preferably formed on a single substrate using 0.18 um CMOS technology or smaller. However, the scope of the invention includes forming the integrated circuit in a multi-chip module.

[0011] The multi-port communications chip 20 may preferably be coupled between a high speed bus 30 and peripheral

components including high speed network devices (not shown) and high speed storage devices 36. The high speed bus 30 couples input/output (I/O) devices to the computer system core components through the core chipset 22. The system core components may include a processor 21, memory 23, and graphics 25. The core chipset 22 may include a bus controller 27 within an I/O bridge 29 to control the flow of information between the high speed bus 30 and the system core components. The high speed bus 30 may comply with any high speed bus standard including HyperTransport™, PCI-X (Peripheral Component Interconnect-Extended), 3GIO (Third Generation Input/Output), and Infiniband™.

[0012] The multi-port communications chip 20 preferably includes a single bus interface 28 to interface to the high speed bus 30. However, another bus interface may be included to interface to the core chipset 22 through another high speed bus. The bus interface includes interfaces such as HyperTransport™ interfaces, PCI-X interfaces, 3GIO interfaces, and Infiniband™ interfaces.

[0013] A high speed Ethernet controller 33 preferably including a MAC (media access control) layer 32 and a physical layer 34 is coupled to the bus interface 28 to provide control functions for network devices (not shown) connected to the network port 26. The MAC layer 32 and physical layer 34 of

the multi-port communications chip 20 are preferably used in conjunction with devices that supply the remainder of Ethernet controller functionality. The high speed Ethernet controller may have an operating speed of 1 Giga Bit or higher.

[0014] A serial ATA host adapter 36 may be coupled between the bus interface 30 and the serial ATA port 24. The serial ATA host adapter 36 connects the core chipset 22 and processor to a storage device 38 that may include a drive controller (not shown). The serial ATA host adapter 36 provides scalable performance starting at 1.5 gigabits per second, and software compatibility with conventional operating systems. Alternatively, the serial ATA host adapter 36 may couple to the core chipset 22 through another bus interface (not shown) and high speed bus. The storage device 38 includes devices such as hard drives, CD-ROM drives, DVD drives, CD-R/W drives, diskette drives, and tape storage drives.

[0015] Conventional systems typically include a parallel ATA host adapter within the core chipset. In addition, the trend in conventional systems is to integrate an increasing number of functions into fewer semiconductor devices such as the core chipset 22. The present invention recognizes the advantages of not including the serial ATA host adapter 36 in the core chipset 22, but instead including the serial ATA host adapter 36 in the multi-port communications chip 20. Serial

ATA operates at a significantly higher data rate than parallel ATA, making the serial ATA host adapter more suitable for fabrication with mixed-signal CMOS processes than fabrication processes typically employed for the core chipset 22. Including the serial ATA host adapter 36 in the core chipset 22 would potentially increase costs due to more complex fabrication methods and possibly lower yields. Instead, the Serial ATA host adaptor 36 is fabricated in a semiconductor device outside of the core chipset 22, which may result in faster time-to-market, improved yield, and lower cost. In addition, the serial ATA host adaptor 36 is combined with the high speed Ethernet controller 33, a function having similar fabrication requirements, into a single semiconductor device. Combining the serial ATA host adapter 36 and the Ethernet controller 33 into a single semiconductor device may decrease cost by combining functions that have similar fabrication requirements, reduce the required board area, and minimize chip count. Also, in a preferred embodiment, recognizing that a single high speed bus 30 can support both the serial ATA host adaptor 36 and the high speed Ethernet controller 33 through a single bus interface 28, leads to the elimination of a separate bus interface and bus for each function. Older technology buses such as PCI (Peripheral Component Interface) do not have sufficient bandwidth on a single bus to adequately

support both a storage device and network controller with present day multimedia requirements. Using a single bus interface 28 to interface both the serial ATA host adaptor 36 and the high speed Ethernet controller 33 to the high speed bus 30 further reduces complexity which may lead to further cost reduction, improved yield, and reduction in required board area.

[0016] Figure 3 shows one embodiment of a high speed Ethernet physical layer device 40. The physical layer device 40 includes four channels 42 each operating at 250 MBits per second. Each of the channels 42 include in the transmit path a waveshape filter 44 coupled to a digital-to-analog converter 46. The receive path includes an active hybrid gain control baseline 48, analog-to-digital converter (A/D) 50, skew control 52, and feed forward equalizer 54 connected in series. An echo canceller 56 and crosstalk canceller 58 are coupled from the transmit path to the receive path. A timing control circuit 60 controls the timing of the A/D 50. A transmit circuit 62, receive circuit 64, and decision feedback equalizer 66 communicate with each of the channels 42.

[0017] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit

and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.